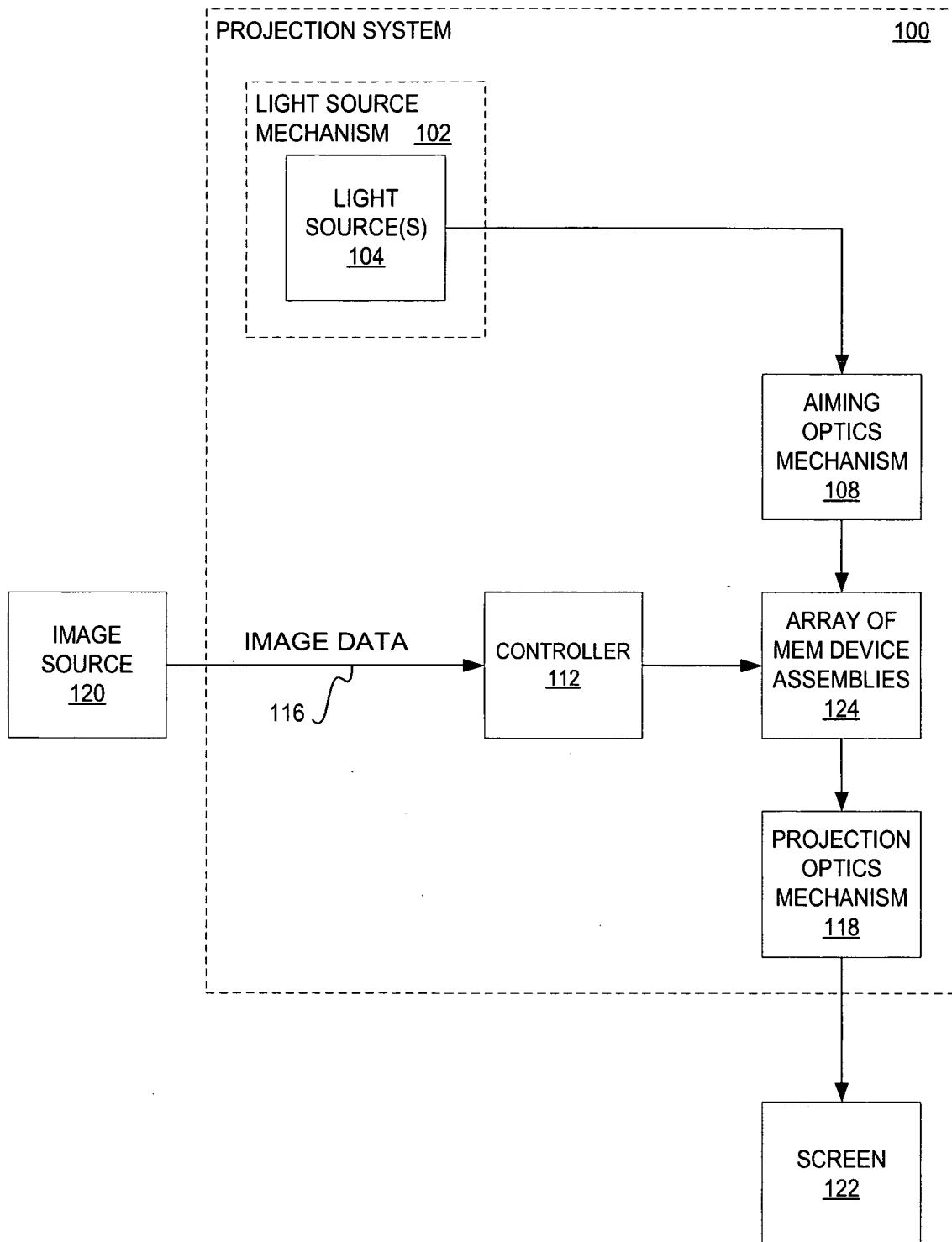


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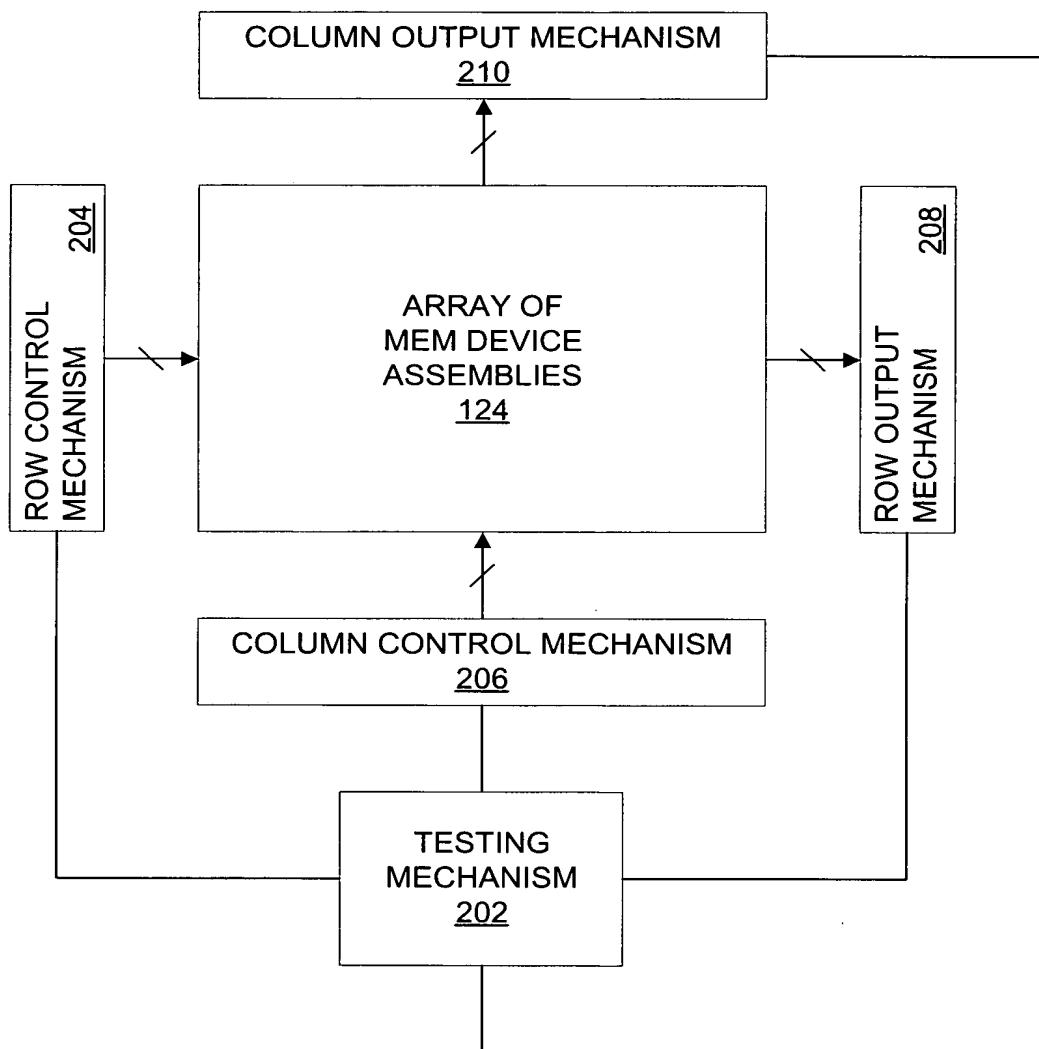
FIG 1



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FIG 2

100



The diagram illustrates a memory device assembly 300. A vertical line represents a COLUMN 328, and a horizontal line represents a ROW 330. The assembly contains a crossbar array of access transistors. Each access transistor is formed by a horizontal access transistor gate 302 and a vertical access transistor gate 312. The access transistors are connected to the COLUMN 328 and ROW 330 lines. A memory device 306 is connected to the access transistors. The diagram also shows a word line 304, a bit line 314, and a sense line 318. The access transistors are labeled 310, 316, and 318. The memory device is labeled 306. The word line is labeled 304. The bit line is labeled 314. The sense line is labeled 318. The access transistor gates are labeled 302 and 312. The access transistor gates are labeled 310, 316, and 318. The access transistor gates are labeled 310, 316, and 318. The access transistor gates are labeled 310, 316, and 318.

FIG 4

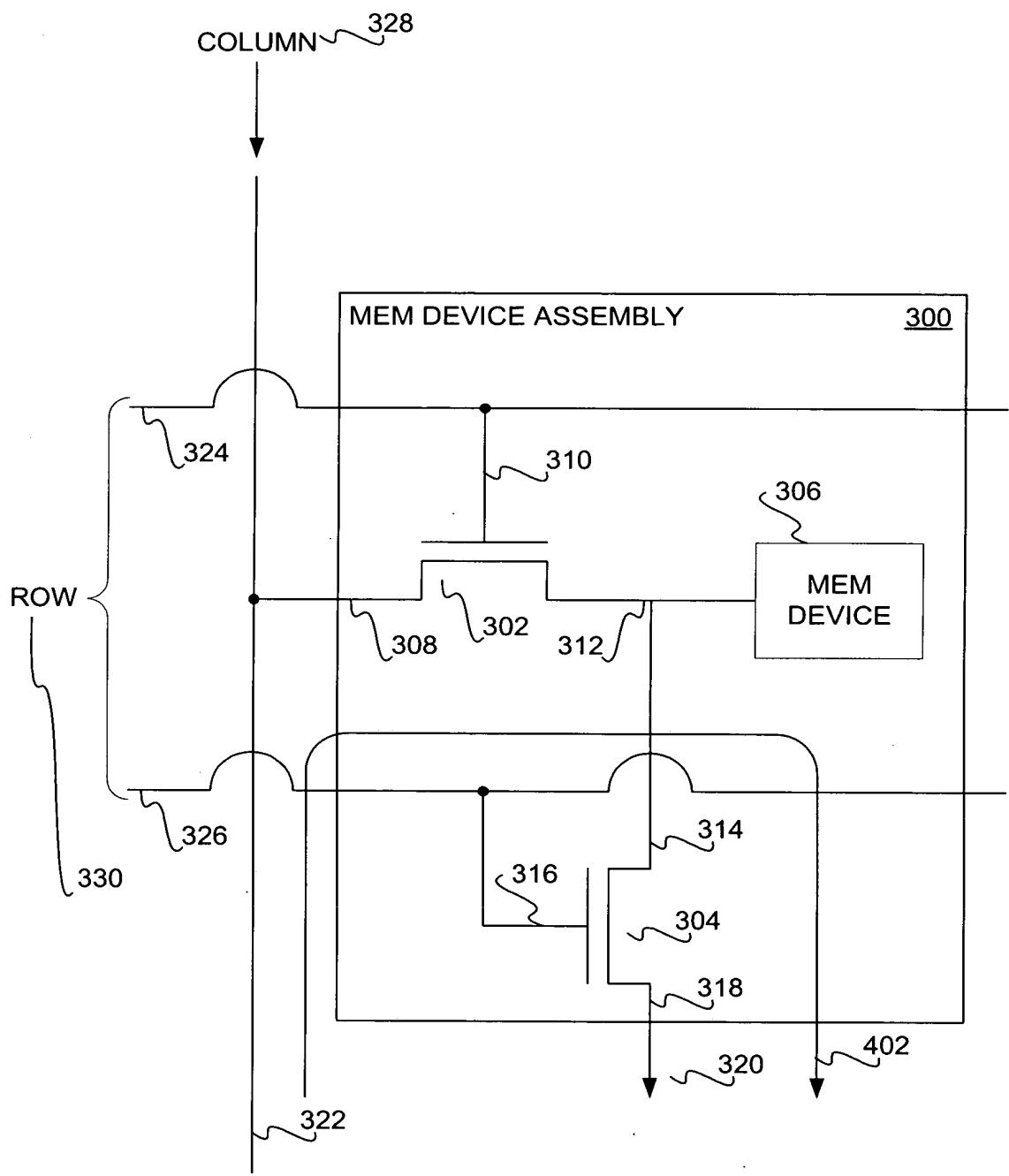


FIG 5

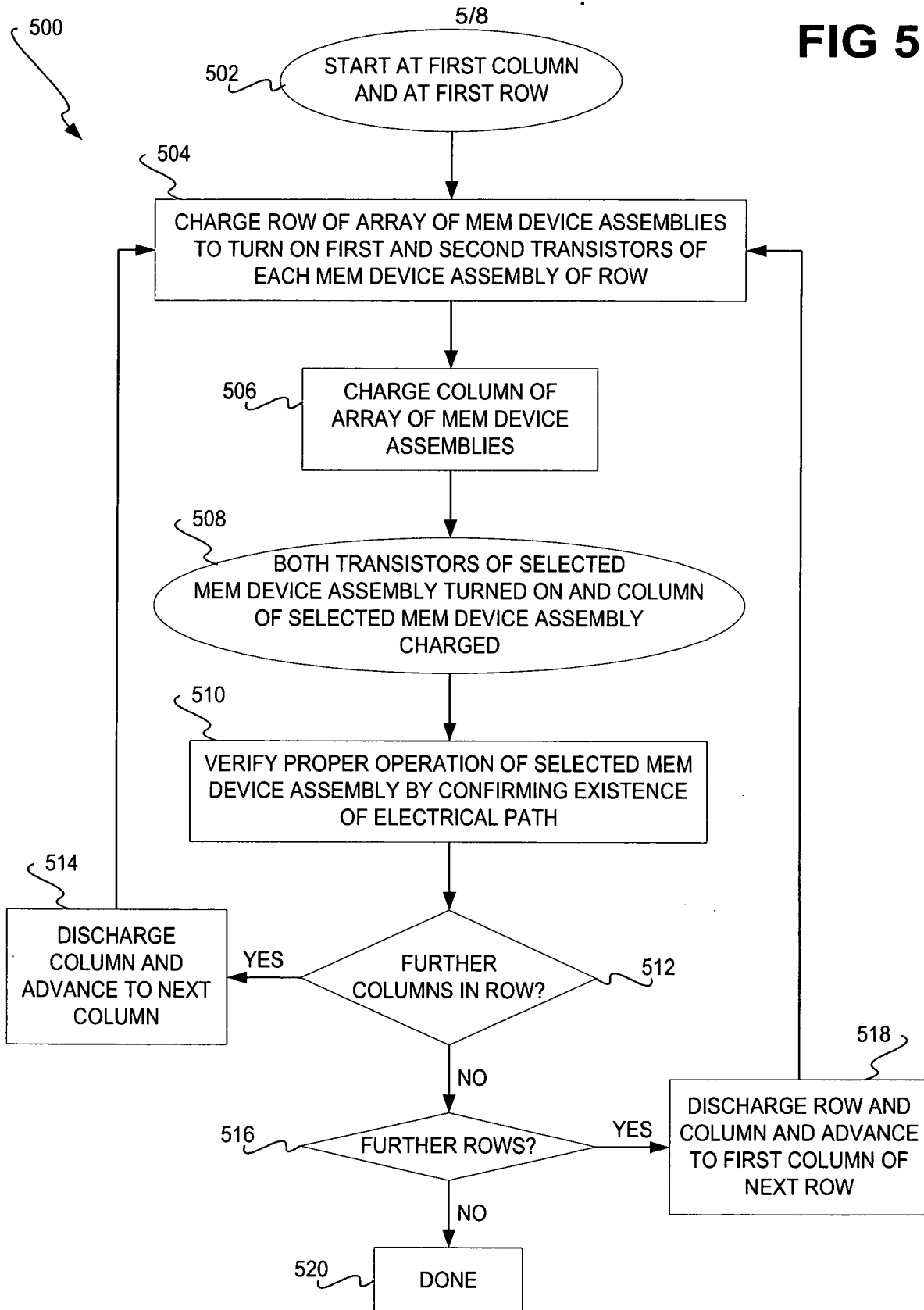
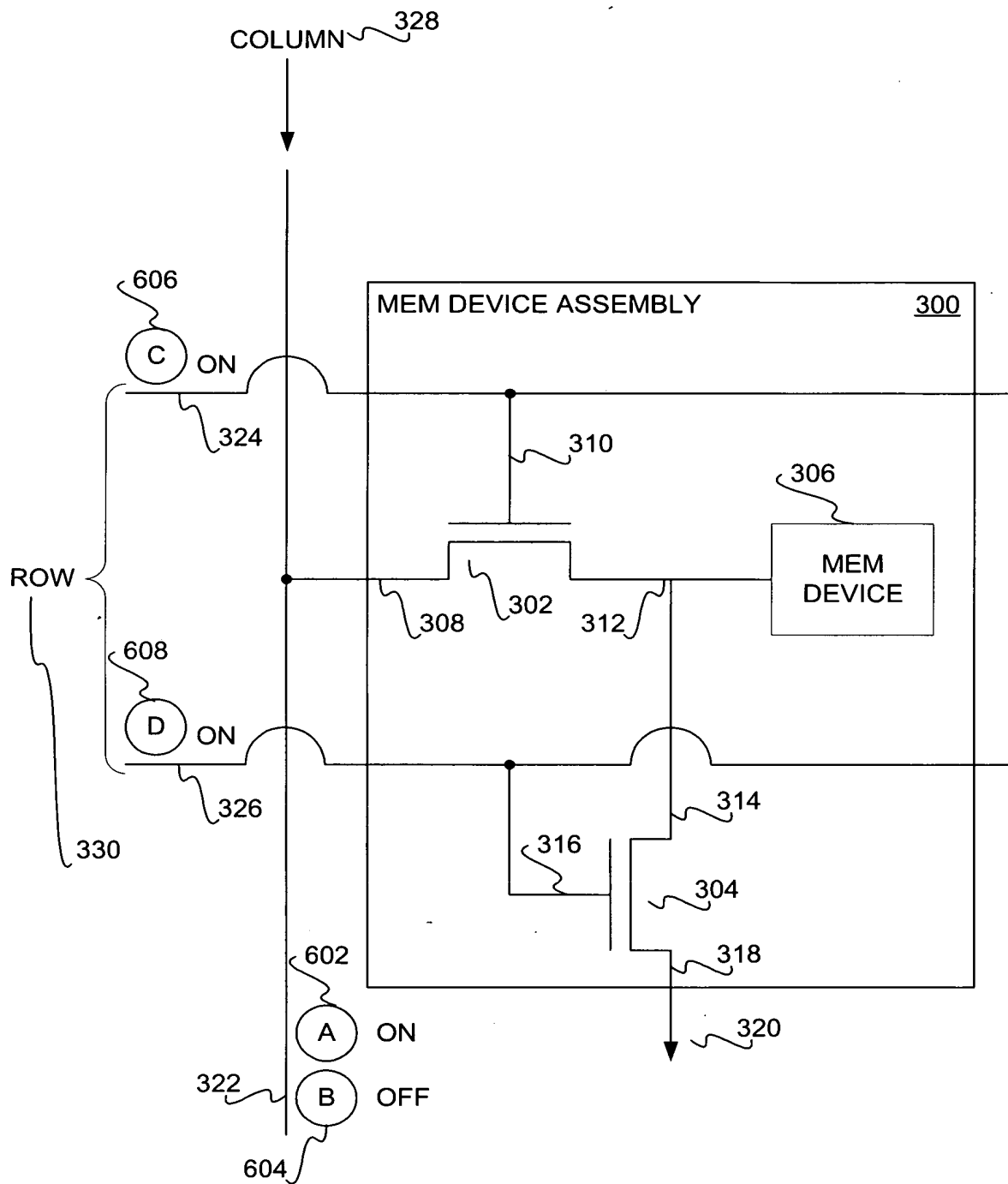


FIG 6



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FIG 7

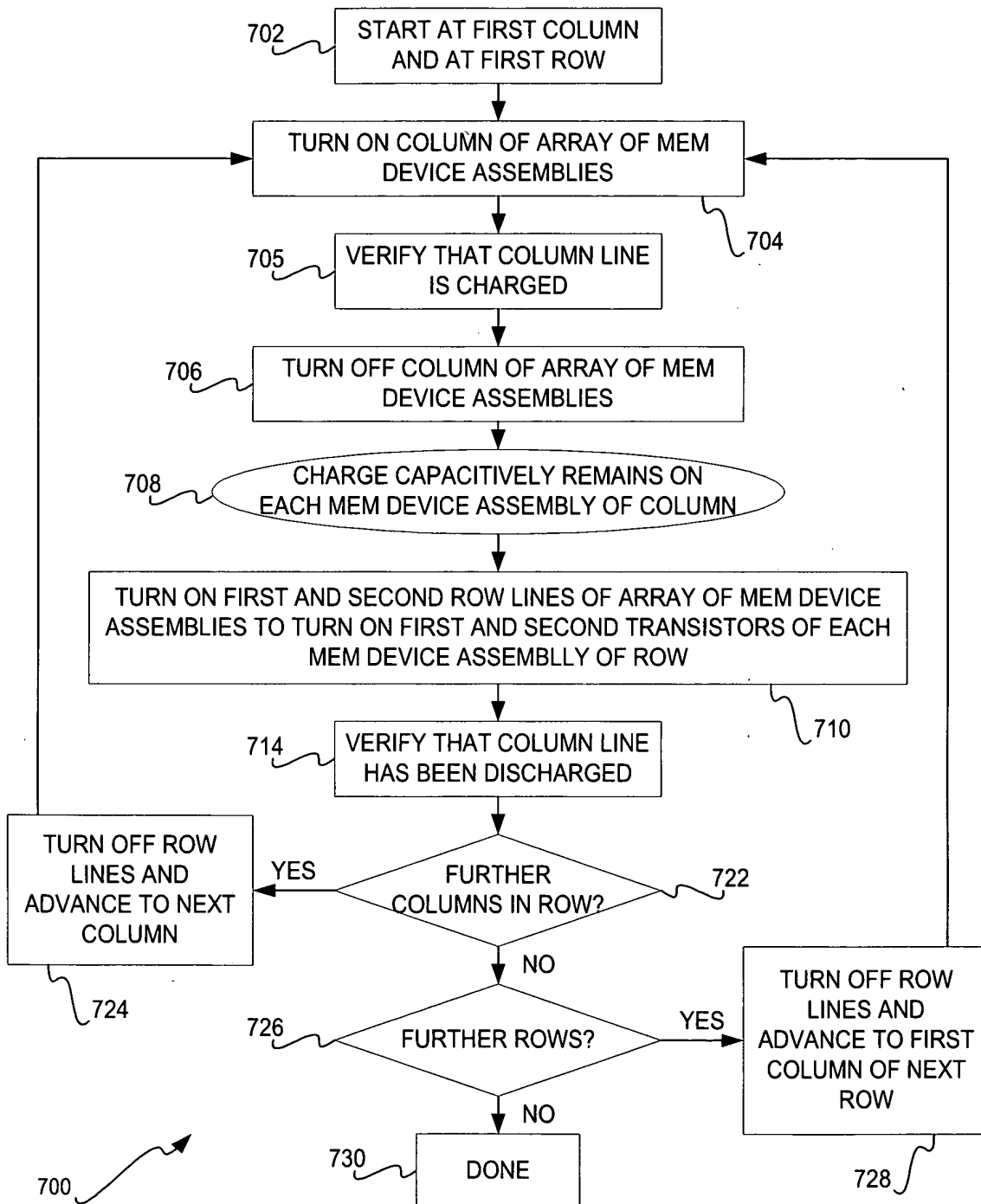


FIG 8

